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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/878,554	06/11/2001	Xinghao Chen	FIS920010060US1	5168

34313 7590 05/04/2005

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/878,554	CHEN ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,6 and 8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,6 and 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 2, 6 and 8-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites the limitation "the potential faults" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim 2 recites the limitation "the faults to be tested" in line 11. There is insufficient antecedent basis for this limitation in the claim. Note it is not clear whether "the faults to be tested" in line 11 refers to "the potential faults to be tested" in line 6 or to "the faults to be tested" in line 1.

Claim 8 recites the limitation "the faults" in line 11. There is insufficient antecedent basis for this limitation in the claim. Note it is not clear whether "the faults" in line 11 refers only to the "potential faults" in line 6 or whether it includes the "fault to be tested" in line 1.

Claim 9 recites the limitation "the faults" in line 13. There is insufficient antecedent basis for this limitation in the claim. Note it is not clear whether "the faults" in line 13 refers only to the "potential faults" in line 8 or whether it includes the "fault to be tested" in line 3.

Claim 8 recites the limitation "the faults" in line 16. There is insufficient antecedent basis for this limitation in the claim. Note it is not clear whether "the faults" in line 16 refers only to the "potential faults" in lines 9-10 or whether it includes the "fault to be tested" in line 3.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2, 6, 8 and 11 rejected under 35 U.S.C. 102(b) as being anticipated by Abramovici; Miron et al. (US 5896401 A, hereafter referred to as Abramovici).

35 U.S.C. 102(b) rejection of claim 2.

Abramovici teaches a) performing a good machine simulation on the IC with the test to obtain values of each internal node of the IC (Fault-Free Circuit 125 in Figure 5 of Abramovici is a good machine simulation on the IC which is included in the Fault Simulation device of Figure 5 for performing a good machine simulation on the IC with the test to obtain values 127 of each internal node of the IC transmitted to Backward Network 115); b) based on the good machine simulation, identifying the potential faults to be tested by the test by backtracing (col. 5, lines 39-52 in Abramovici teaches that backtracing is performed by the to Backward Network 115 in Figure 5 of Abramovici

based on values 127 received from good machine simulation Fault-Free Circuit 125; the Abstract in Abramovici teaches that backtracing in the Backward Network 115 is used for computing critical paths, the critical paths indicating faults; hence Abramovici teaches backtracing in the Backward Network 115 is used for computing critical paths for identifying potential faults; Note: the abstract in Abramovici teaches that critical paths are paths with faults that are detectable by the input test signals, hence are potential faults to be tested), in a single detection pass, through logic gates and memory elements starting at each observable node (See Figure 12 in Abramovici), said backtracing being based on said good machine simulation (col. 5, lines 39-52 in Abramovici teaches that backtracing is performed by the to Backward Network 115 in Figure 5 of Abramovici based on values 127 received from good machine simulation Fault-Free Circuit 125) and being limited to paths along which a faulty value has a possibility of propagating to said observable node (Note: the abstract in Abramovici teaches that critical paths are paths with faults that are detectable by the input test signals, hence are potential faults to be tested); c) with the test, performing the fault simulation on the faults to be tested (the Fault Simulation device of Figure 5 of Abramovici performs fault simulation on the inserted faults to be tested received on line 129 from Backward Network 115); and d) repeating a) through c) for additional tests of the plurality of tests (col. 5, lines 4-8 of Abramovici teach that a test for each test vector "t" is performed hence Abramovici teaches repeating a) through c) for additional tests of the plurality of tests).

35 U.S.C. 102(b) rejection of claim 6.

Col. 6, lines 37-52 in Abramovici teaches observed results of stem analysis during the test further limit a number of faults requiring processing by the fault simulation by recognizing that is not always necessary to propagate the fault effects of stems "all the way" to POs and by starting the backtraces from only observable nodes wherein the faults to be tested were detected, for example, from node F as taught in col. 6, lines 37-52 of Abramovici.

35 U.S.C. 102(b) rejection of claim 8.

Abramovici teaches a) performing a good machine simulation on the IC with the test to obtain values of each internal node of the IC (Fault-Free Circuit 125 in Figure 5 of Abramovici is a good machine simulation on the IC which is included in the Fault Simulation device of Figure 5 for performing a good machine simulation on the IC with the test to obtain values 127 of each internal node of the IC transmitted to Backward Network 115); b) based on the good machine simulation, identifying the potential faults to be tested by the test by backtracing (col. 5, lines 39-52 in Abramovici teaches that backtracing is performed by the to Backward Network 115 in Figure 5 of Abramovici based on values 127 received from good machine simulation Fault-Free Circuit 125; the Abstract in Abramovici teaches that backtracing in the Backward Network 115 is used for computing critical paths, the critical paths indicating faults; hence Abramovici teaches backtracing in the Backward Network 115 is used for computing critical paths for identifying potential faults; Note: the abstract in Abramovici teaches that critical paths

are paths with faults that are detectable by the input test signals, hence are potential faults to be tested), in a single detection pass, through logic gates and memory elements starting at each observable node (See Figure 12 in Abramovici), said backtracing being based on said good machine simulation (col. 5, lines 39-52 in Abramovici teaches that backtracing is performed by the to Backward Network 115 in Figure 5 of Abramovici based on values 127 received from good machine simulation Fault-Free Circuit 125) and being limited to paths along which a faulty value has a possibility of propagating to said observable node (Note: the abstract in Abramovici teaches that critical paths are paths with faults that are detectable by the input test signals, hence are potential faults to be tested); c) with the test, performing the fault simulation on the faults to be tested (the Fault Simulation device of Figure 5 of Abramovici performs fault simulation on the inserted faults to be tested received on line 129 from Backward Network 115); and d) repeating a) through c) for additional tests of the plurality of tests (col. 5, lines 4-8 of Abramovici teach that a test for each test vector "t" is performed hence Abramovici teaches repeating a) through c) for additional tests of the plurality of tests). Note: critical paths are paths with faults that are not blocked from being observed at an observable point.

35 U.S.C. 102(b) rejection of claim 11.

Col. 6, lines 37-52 in Abramovici teaches observed results of stem analysis during the test further limit a number of faults requiring processing by the fault simulation by recognizing that is not always necessary to propagate the fault effects of stems "all the

way" to POs and by starting the backtraces from only observable nodes wherein the faults to be tested were detected, for example, from node F as taught in col. 6, lines 37-52 of Abramovici.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 9, 10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abramovici; Miron et al. (US 5896401 A, hereafter referred to as Abramovici).

35 U.S.C. 103(a) rejection of claim 9.

Claim 9 is a software implementation of the limitations in claim 8 containing all of the limitations of claim 8 except for the software implementation of those limitations.

Abramovici, substantially teaches the claimed invention described in claim 8 (as rejected above).

However Abramovici, does not explicitly teach the specific use of a software implementation for the limitations in claim 8.

The Examiner asserts that use of a software implementation for the limitations in claim 8 versus a hardware implementation for the limitations in claim 8 or any combination thereof would have been based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is generally faster than software) and flexibility (Note: software is more flexible than hardware).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Abramovici by including use of a software implementation for the limitations in claim 8. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a software implementation for the limitations in claim 8 would have provided the opportunity to implement the test device in the Abramovici patent based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is generally faster than software) and flexibility (Note: software is more flexible than hardware).

35 U.S.C. 103(a) rejection of claim 10.

Claim 10 is a software implementation of the limitations in claim 8 containing all of the limitations of claim 8 except for the software implementation of those limitations. Abramovici, substantially teaches the claimed invention described in claim 8 (as rejected above).

However Abramovici, does not explicitly teach the specific use of a software implementation for the limitations in claim 8.

The Examiner asserts that use of a software implementation for the limitations in claim 8 versus a hardware implementation for the limitations in claim 8 or any combination thereof would have been based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is generally faster than software) and flexibility (Note: software is more flexible than hardware).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Abramovici by including use of a software implementation for the limitations in claim 8. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a software implementation for the limitations in claim 8 would have provided the opportunity to implement the test device in the Abramovici patent based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is generally faster than software) and flexibility (Note: software is more flexible than hardware).

35 U.S.C. 103(a) rejection of claim 12.

Col. 6, lines 37-52 in Abramovici teaches observed results of stem analysis during the test further limit a number of faults requiring processing by the fault simulation by recognizing that is not always necessary to propagate the fault effects of stems "all the way" to POs and by starting the backtraces from only observable nodes wherein the faults to be tested were detected, for example, from node F as taught in col. 6, lines 37-52 of Abramovici.

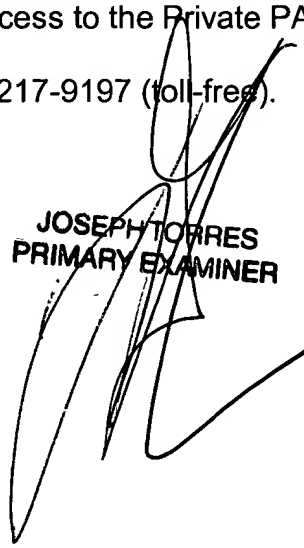
35 U.S.C. 103(a) rejection of claim 13.

Col. 6, lines 37-52 in Abramovici teaches observed results of stem analysis during the test further limit a number of faults requiring processing by the fault simulation by recognizing that is not always necessary to propagate the fault effects of stems "all the way" to POs and by starting the backtraces from only observable nodes wherein the faults to be tested were detected, for example, from node F as taught in col. 6, lines 37-52 of Abramovici.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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Art Unit 2133